

# Sandeep Chris Ramlochan

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## Education

### Rice University

May 2028

B.S. Electrical and Computer Engineering · GPA: 3.80 · Minors: Engineering Design, Mathematics

**Coursework:** VLSI System Design, Advanced VLSI Design, Computer Architecture, Embedded Systems, Signal Processing.

## Leadership & Program Management

### NeoFeed (Patent Pending) | *Co-Founder & Hardware Lead*

Aug 2024 – Present

- Defined project plans and led execution across 3 prototype revisions for a neonatal feeding monitor, coordinating electrical engineering, firmware, clinical research, and regulatory workstreams on parallel timelines (neofeedhealth.com).
- Coordinated validation with 12 neonatal nurses across 8 hospitals in the Dominican Republic; resolved hardware-clinical interdependencies by translating sensor performance data into language bedside staff could act on.
- Managed the regulatory pathway end-to-end: secured IRB approval at Parkland Health, filed a provisional patent for the sensor coupling method, and scoped the FDA 510(k) submission with clinical partners at UTHealth Houston.
- Presented technical status, schedule risks, and design trade-offs to hospital administrators and university stakeholders with no engineering background; adjusted scope and priorities based on clinical feedback without slipping milestones.

### Rice Wind Energy Club | *Controls Lead*

2025 – Present

- Led a cross-functional subteam spanning mechanical, electrical, and software engineers; set weekly milestones, tracked deliverables, and facilitated integration across disciplines to keep the project on schedule.
- Identified and resolved conflicting technical dependencies between the controls and structures teams, preventing a 2-week slip in the test timeline.

### Sempionatto Lab, Rice University | *Wearables Hardware Intern*

May 2025 – Aug 2025

- Coordinated across 3 workstreams (electrochemistry, mixed-signal PCB, machine learning) to deliver an end-to-end biosensor wearable prototype within a 10-week timeline; owned the PCB architecture and integration schedule.
- Built a Python HIL validation suite that cut debug cycles by 40%, unblocking faster iteration for 4 other researchers on the team.
- Presented final results (blood glucose prediction model:  $R^2 = 0.92$ , RMSE = 18.5 mg/dL) at the Rice summer research symposium.

### Fondren Library, Rice University | *Services Desk*

2023 – Present

- Managed competing requests from students and faculty during peak hours; resolved issues calmly under time pressure while maintaining organized service operations.

## Technical Project Experience

### Tetris ASIC | *ELEC 422, Rice University*

Spring 2026

- Took a custom ASIC from RTL through GDSII (Design Compiler, Innovus, Magic, IRSIM): managed the full design schedule, tracked milestones across synthesis, P&R, and verification, and delivered a working design (20 MHz / 6,056 cells / 28.7 mW) with zero post-synthesis regression.

### Pipelined RISC-V Processor | *VLSI & Computer Architecture*

Spring 2026

- Designed a 5-stage pipelined RV32I processor in Verilog; optimized the ALU critical path for a 15% frequency improvement and wrote a constrained-random verification suite to catch corner-case instruction bugs.

### Autonomous Self-Driving RC Car | *ELEC 424, Rice University*

Spring 2026

- Led a 4-person team building a lane-following car on RPi 5 with OpenCV, PD control, and real-time YOLOv5 at 25+ FPS; divided workstreams across vision, controls, and firmware and delivered a working demo on schedule.

### High-Altitude Balloon Telemetry | *Project Engineer*

Fall 2024

- Planned and launched an electronics payload above 30 km: owned the hardware BOM, assembly schedule, and flight-day logistics. Custom PCB with TI MCU, GPS, barometric/temp sensors, flash logging, and radio telemetry.

### Low-Power Sensor Interface Controller | *Tiny Tapeout (SKY130)*

Summer 2026

- Designed a sensor hub in Verilog on the Skywater 130 nm PDK; ran the full OpenLane flow from synthesis through DRC/LVS signoff and submitted GDS for fabrication.

### TRACE | *AI Circuit Design Scratchpad*

2025

- Built a tool that turns plain-English circuit descriptions into rough schematics with live DigiKey BOM pricing (Flask + Anthropic API).

## Skills

**Program Management:** Project planning, cross-functional coordination, schedule tracking, stakeholder communication, risk identification, regulatory navigation.

**Technical:** Verilog, SystemVerilog, PCB design, C/C++, Python, Design Compiler, Innovus, STM32, I2C/SPI, test automation.