

# ELEC 422

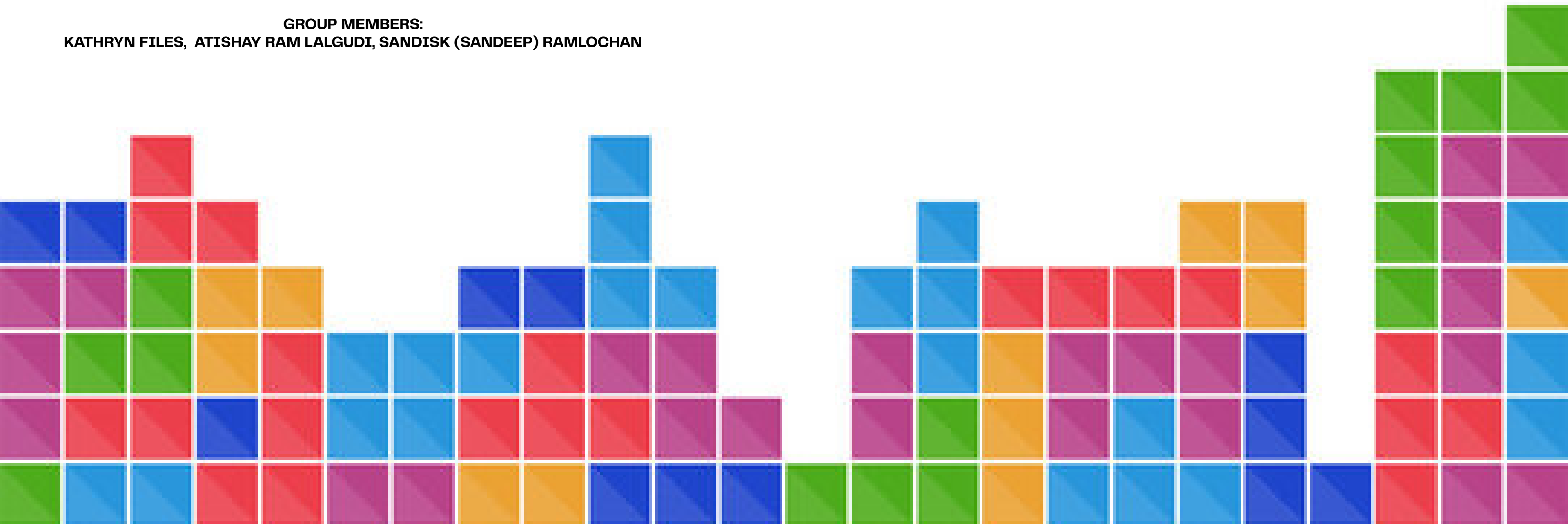


RICE

# TETRIS ASIC

**TEAM NAME:**  
MEMORY MAFIA

**GROUP MEMBERS:**  
KATHRYN FILES, ATISHAY RAM LALGUDI, SANDISK (SANDEEP) RAMLOCHAN

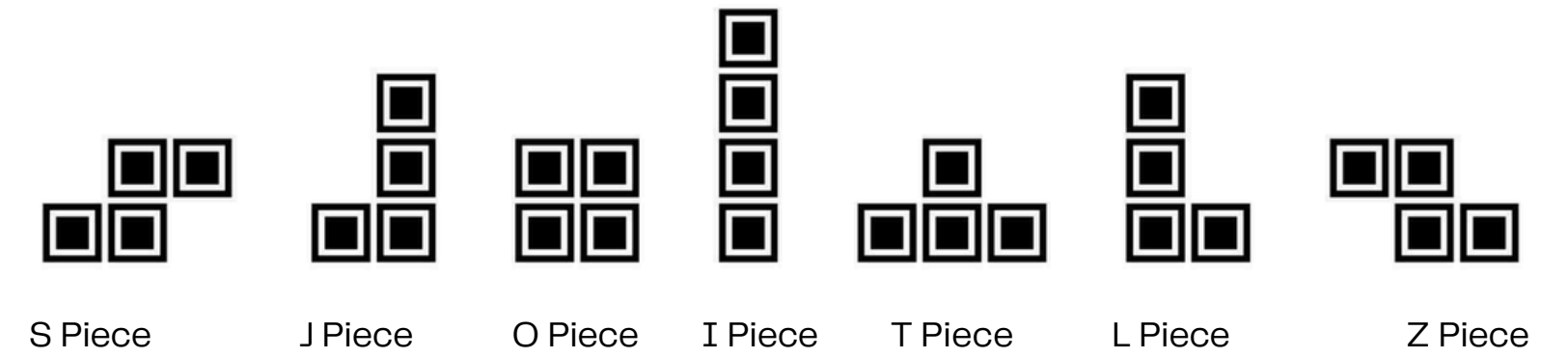


# OVERVIEW

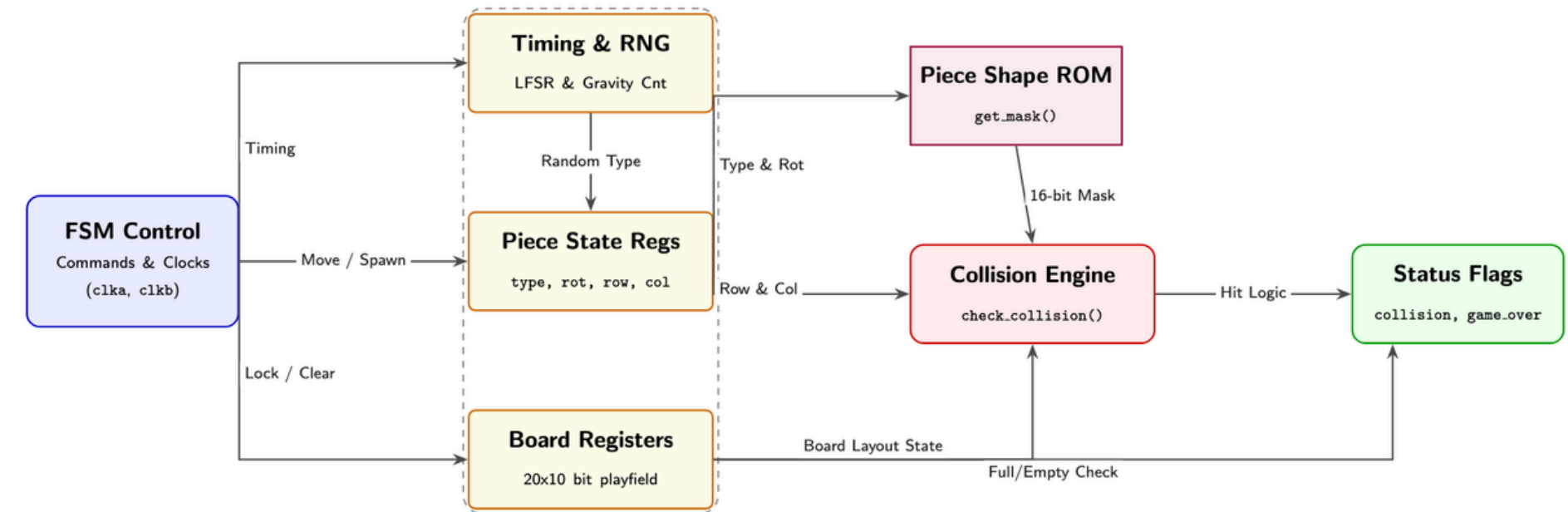
The goal of this project was to design an ASIC-level Tetris logic core optimized for a 61-pin Integrated Circuit (IC) environment.

Unlike a software-based game, this design operates as a synchronous digital system that directly manipulates hardware registers to represent the game state.

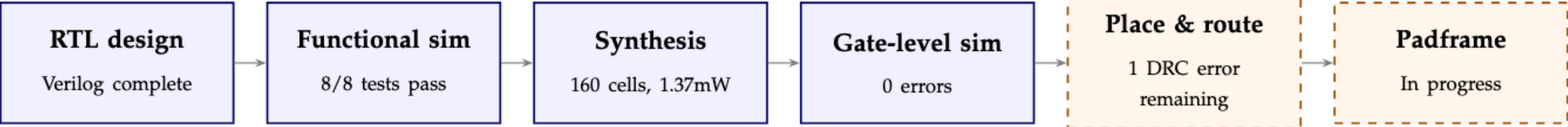
To minimize complexity and gate count, the system avoids high-level video signals (VGA/HDMI) in favor of a row-by-row bit-mapped output, suitable for driving an LED matrix or a terminal-based bit-renderer.



The system manages seven standard tetromino shapes within a bit-mapped grid.



# STATUS AND ISSUES (RESOLVED!)



Verilog HDL  
Controller/Datapath  
architecture, two-  
phase non  
overlapping clock

Questa sim  
All 8 testbenches  
pass movement,  
collision, row clear,  
scoring, game over

Synopsys DC  
160 standard  
cells, 1.37 mW,  
7.21 ns slack on  
10 ns period

Questa sim  
Post-synthesis netlist  
verified: timing and  
logic match RTL  
exactly

Cadence Innovus  
0 DRC

Magic  
61-pin DIP  
mapping defined,  
I/O padframe  
integration  
finished



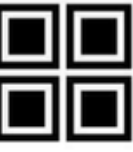
S Piece

■ Complete



J Piece

■ Complete



O Piece

■ Complete



I Piece

■ Complete



T Piece

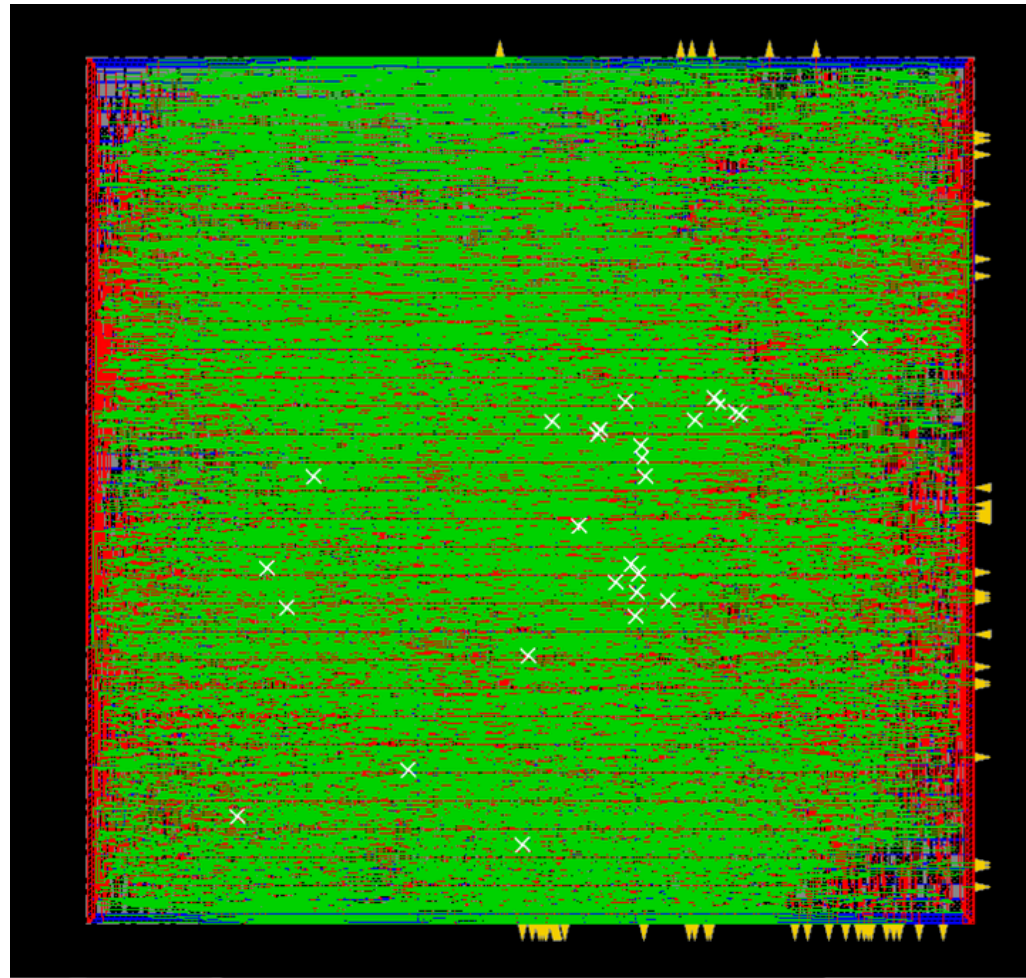
Complete



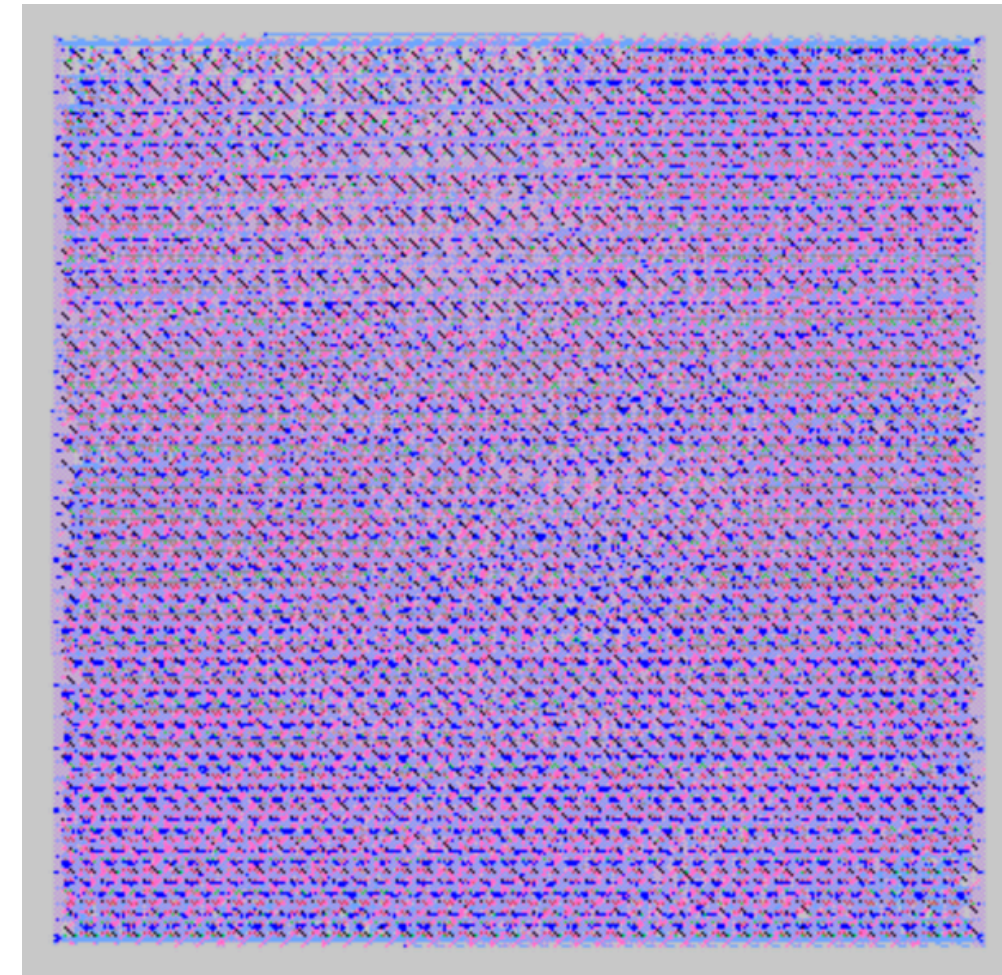
Z Piece

■ Complete

# CHIP SYNTHESIS AND LAYOUT

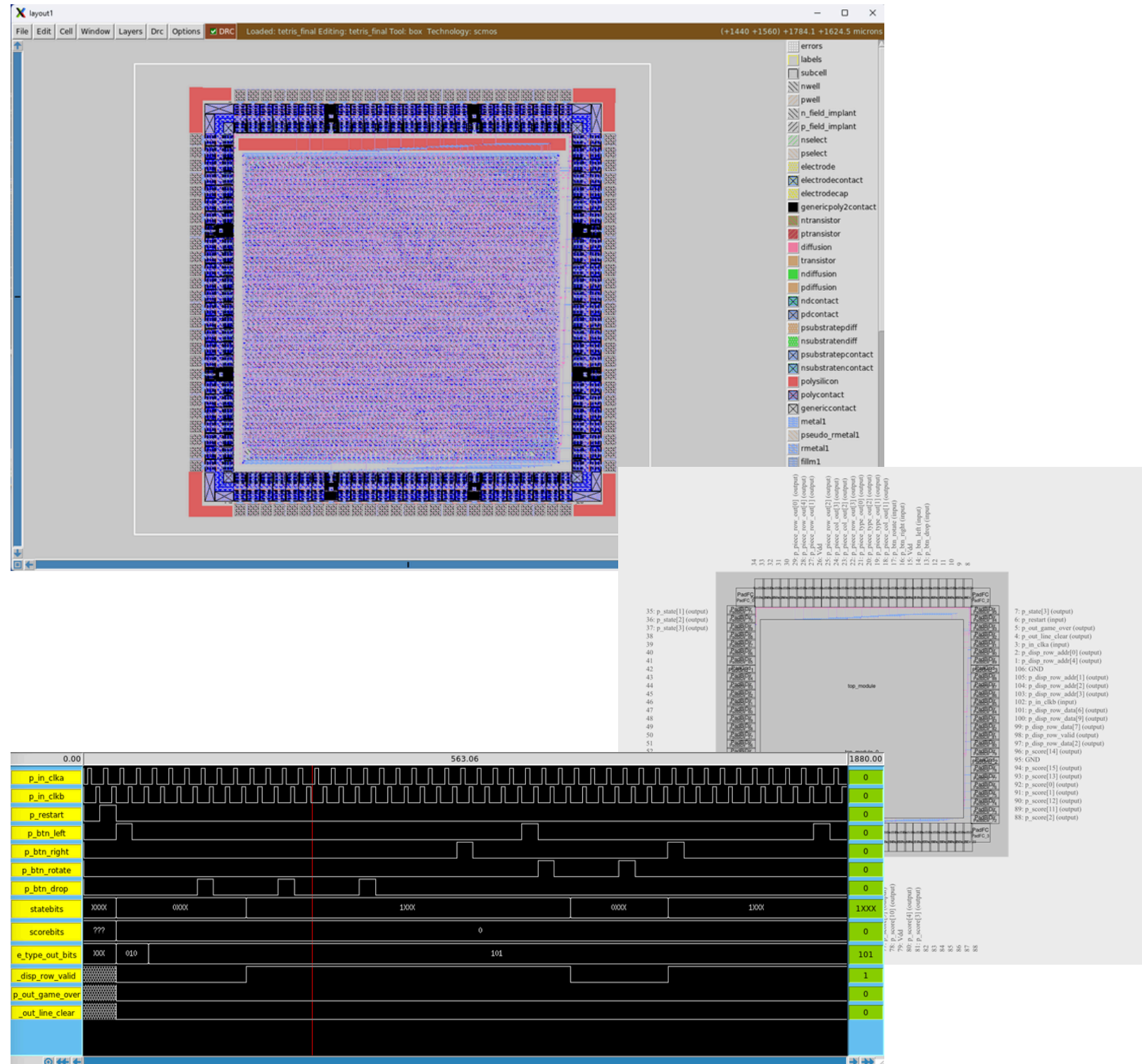


**INNOVUS**



**MAGIC**  
GDS READ TETRIS.GDS

# PADFRAME INTEGRATION



Core size:  $7319 \times 7140 \lambda$

Initial Pad Frame ( 64 pads) size:  $4,600 \times 4,600 \lambda$

Custom padframe interior:  $7,200 \times 7,200 \lambda$

104 pads total: 88 signal, 6 VDD, 6 GND, 4 corner

57 core ports mapped

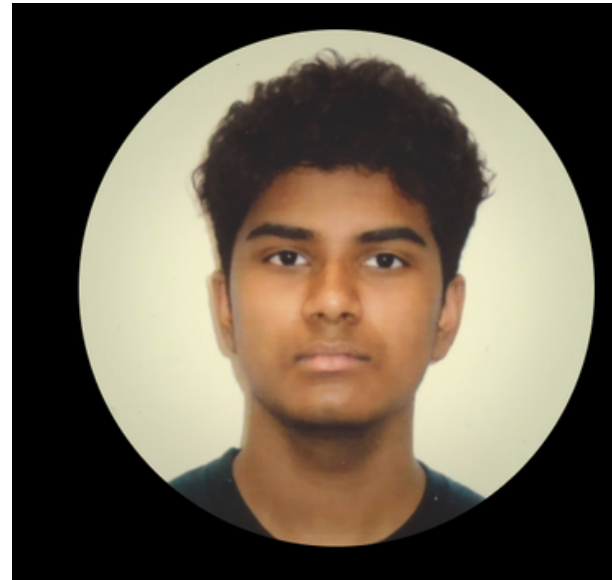
Tool: Magic + cell\_placement.py (Gavin Jing)

Signal Routing Finished!

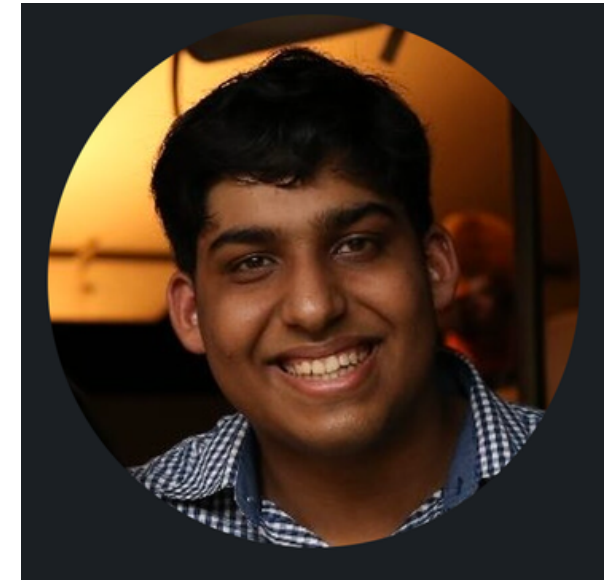
# TEAM



Kathryn Files



Atishay Lalgudi



Sandeep Ramlochan

Logic and verilog files designed as a team  
Each team member did a Magic process (for fsm, data path, and integration with top module)  
Debugging integrated magic design as a team